CLAIMS

Please amend the claims as follows:

1-27. (Canceled)

28. (Currently Amended): A method for implementing a phase-locked loop comprising:

connecting a detector differentially to a transconductance cell, the detector having a first differential input port responsive to a differential input signal and a second differential input port responsive to a differential feedback signal;

connecting the transconductance cell differentially to a signal filter;

connecting the signal filter differentially to a voltage controlled oscillator;

connecting the voltage controlled oscillator differentially to the second differential input port of the ~~differential~~ detector through a differential divider; and

implementing the phase-locked loop using ~~the~~ current-controlled CMOS logic.

29. (Currently Amended): The method of implementing [[a]] the phase-locked loop of claim 28, wherein the detector [[is]] includes a differential phase-frequency detector.

30. (Currently Amended): The method of implementing [[a]] the phase-locked loop of claim 28, wherein the signal filter [[is]] includes a differential lowpass filter.

31. (Currently Amended): The method of implementing [[a]] the phase-locked loop of claim 28, wherein the detector includes:

a first resetable flip-flop configured to receive the differential input signal;

a second resetable flip-flop configured to receive the differential feedback signal[[ ]];

an AND logic function component configured to receive differential outputs from the first resetable flip-flop and the second resetable flip-flop; and

one or more buffers configured to receive output from said AND logic function component and to provide a reset signal to reset the first resetable flip-flop and the second resetable flip-flop.